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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,827	11/13/2003	Jun Koyama	12732-176001	7838
26171	7590	08/14/2007	EXAMINER	
FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			LAO, LUN YI	
		ART UNIT	PAPER NUMBER	
		2629		
		MAIL DATE	DELIVERY MODE	
		08/14/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/705,827	KOYAMA ET AL.
	Examiner	Art Unit
	LUN-YI LAO	2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 20 June 2007.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-44 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 13 November 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 3/29/2007.
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application
- 6) Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-44 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-28 of U.S. Patent No. 7,027,0740 in view of Nishioka et al(5,390,293) and Kuwajima et al(6,339,422).

The US patent teach a display comprising a first means for diving one frame period into a plurality of subframe periods and expressing n-bits gradation(n is natural number of two or more) in accordance with a total lighting time during a frame period and second means not for dividing one frame period into a plurality of subframe periods and second means for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a total lighting time during the one

frame period, and for operating the display with a lower clock frequency than the first means (see claims 1-16).

The US patent fails to disclose a frame period in 1-bit gradation mode having a longer frame period than the n-bits gradation and second means having a lower driving voltage or current than the first means.

Nishioka et al teach a frame period(60HZ= 16.7 ms) in less bits(e.g. 3 bits, 512 RGB color) gradation mode having a longer frame period than the larger bits gradation(e.g. 4 bits, 4096 RGB color, 80HZ=12.5 ms)(see figures 1, 4-14; column 2, lines 25-47; column 4, lines 21-59; column 9, lines 1-39; column 18, lines 32-61 and column 26, lines 34-39). It would have been obvious to have 1-bit gradation since N could be any integer number(see column 3, lines 20-29). It would have been obvious to have modified the US patent with the teaching of Nishioka et al, so as to save power(see column 5, lines 13-23).

Kuwajima et al teach a voltage applied to the pixel element in the frame period of the first display mode is higher than in the frame period of the second display mode(see figures 2-3; column 7, lines 66-68 and column 8, lines 1-6). It would have been obvious to have modified the US patent with the teaching of Kuwajima et al, since more gray scale level need more voltage.

As to claims 7, 8, 16, 26-27 and 35, it would have been obvious to have a current supplied to the pixel element in the frame period of the first display mode is larger than frame period of the second display mode since Kuwajima et al teach a voltage applied to the pixel element in the frame period of the first

display mode is higher than in the frame period of the second display mode(see figures 2-3; column 7, lines 66-68 and column 8, lines 1-6) and the current will increased when the voltage is increase.

3. Claims 1-44 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-26 of copending Application No. 10/385,712 in view in view of Nishioka et al(5,390,293) and Kuwajima et al(6,339,422).

The copending application(10/385,712) teaches a display comprising a first means for diving one frame period into a plurality of subframe periods and expressing n-bits gradation(n is natural number of two or more) in accordance with a total lighting time during a frame period and second means not for dividing one frame period into a plurality of subframe periods and second means for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a total lighting time during the one frame period, and for operating the display with a lower voltage or current than the first means (see claims 1-26).

The copending application(10/385,712) fail to disclose a frame period in 1-bit gradation mode having a longer frame period than the n-bits gradation and second means having a lower driving voltage or current than the first means.

Nishioka et al teach a frame period(60HZ= 16.7 ms) in less bits(e.g. 3 bits, 512 RGB color) gradation mode having a longer frame period than the larger bits gradation(e.g. 4 bits, 4096 RGB color, 80HZ=12.5 ms)(see figures 1, 4-14; column 2, lines 25-47; column 4, lines 21-59; column 9, lines 1-39; column 18, lines 32-61 and

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column 26, lines 34-39). It would have been obvious to have 1-bit gradation since N could be any integer number(see column 3, lines 20-29). It would have been obvious to have modified the US copending application with the teaching of Nishioka et al, so as to save power(see column 5, lines 13-23).

Kuwajima et al teach a display disclose a second manes for operating display with lower clock frequency(70HZ) than the first means(140HZ)(see figures 2-5 and column 10, lines 10-19). It would have been obvious to have modified the copending application with the teaching of Kuwajima et al, so as to save power when the display operated in a binary display.

4. Claims 1-44 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-27 of copending Application No. 11/419,345 in view in view of Nishioka et al(5,390,293).

The copending application teach a display comprising a first means for diving one frame period into a plurality of subframe periods and expressing n-bits gradation(n is natural number of two or more) in accordance with a total lighting time during a frame period and second means not for dividing one frame period into a plurality of subframe periods and second means for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a total lighting time during the one frame period, and for operating the display with a lower clock frequency and a lower driving voltage than the first means (see claims 1-27).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10/705,827(claim 1)	11/419,345
a display controller	a display controller
a first means for dividing one frame period into a plurality of subframe periods and setting one of lighting and non-lighting to each of the plurality of subframe periods, and for expressing n-bits gradation (n is a natural number of two or more) in accordance with a total lighting time during the one frame period;	the first display mode, one frame period is divided into a plurality of subframe periods, each of the plurality of subframe periods is either a lighting period or a non-lighting period, and an n-bit (where n is a natural number equal to or more than 2) gray scale is expressed by the sum total of a lighting time within the one frame period,
A second means not for dividing one frame period into a plurality of subframe periods, for setting one of lighting and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a total lighting time during the one frame period, and for operating the display with a lower clock frequency and a lower driving voltage than the first means,	the second display mode, the display is operated by a lower clock frequency and a lower driving voltage than in the first display mode, one frame period is either a lighting period or a non-lighting period, and a one-bit gray scale is expressed by the sum total of a lighting time within the one frame period,

The copending application fail to disclose a frame period in 1-bit gradation mode having a longer frame period than the n-bits gradation.

Nishioka et al teach a frame period(60HZ= 16.7 ms) in less bits(e.g. 3 bits, 512 RGB color) gradation mode having a longer frame period than the larger bits gradation(e.g. 4 bits, 4096 RGB color, 80HZ=12.5 ms)(see figures 1, 4-14; column 2, lines 25-47; column 4, lines 21-59; column 9, lines 1-39; column 18, lines 32-61 and column 26, lines 34-39). It would have been obvious to have 1-bit gradation since N

could be any integer number(see column 3, lines 20-29). It would have been obvious to have modified the US copending application with the teaching of Nishioka et al, so as to save power(see column 5, lines 13-23).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8, 11-16, 19-27, 30-35 and 38-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama(2002-0154151) in view of Nishioka et al(5,390,293)

As to claims 1-8, 11-16, 19-27, 30-35 and 38-44, Koyama teaches a display device comprising: a display; a display controller(102)(see figure 4 and paragraph 227); a first means for dividing one frame period into a plurality of subframe periods(e.g. SF1-SF4) and setting one of lighting and non-lighting to each of the plurality of subframe periods(SF1-SF4); and for expressing n-bits gradation(e.g.n=4) in accordance with a total lighting time during the one frame period; and a second means not for dividing one frame period into a plurality of subframe periods(SF1-SF8), for setting one of lighting

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and non-lighting to the one frame period, for expressing 1-bit gradation in accordance with a total lighting time during the one frame period, and for operating the display with a lower clock frequency than the first means, wherein the first and second means are controlled by the display controller(see figures 1-9 and paragraphs 118, 129, 149, 217-224, 236-247, 251-255, 287 and claim 14).

Koyama fails to disclose a frame period in 1-bit gradation mode having a longer frame period than the n-bits gradation.

Nishioka et al teach a frame period(60HZ= 16.7 ms) in less bits(e.g. 3 bits, 512 RGB color) gradation mode having a longer frame period than the larger bits gradation(e.g. 4 bits, 4096 RGB color, 80HZ=12.5 ms)(see figures 1, 4-14; column 2, lines 25-47; column 4, lines 21-59; column 9, lines 1-39; column 18, lines 32-61 and column 26, lines 34-39). It would have been obvious to have 1-bit gradation since N could be any integer number(see column 3, lines 20-29). It would have been obvious to have modified Koyama with the teaching of Nishioka et al, so as to save power(see column 5, lines 13-23).

As to claims 3-4, 14, 22, 23 and 33, Koyama teaches a display device further comprises a frame memory(105, 106), n-bits data (n is natural number of two or more; e.g. n=4) is written and read out so that display(100) is conducted in the a first means and 1-bit data is written and read out so that display is conducted in the second means(see figures 1-9; paragraphs 217-224, 225-231 and 240-258).

As to claims 5-6, 11, 12, 15, 19, 24-25, 30-31, 34 and 38, Koyama teaches a voltage applied to the light emitting element(804) in the first means is higher than a

voltage applied to the light emitting element in the second means(see figures 1, 8; paragraphs 42, 258 and 262).

As to claims 7-8, 16, 26-27 and 35, Koyama teaches a current supplied to the pixel element in the frame period of the first means is larger than the second means(see figures 1, 8; paragraphs 42, 258, 262 and 265).

As to claims 39-44, Koyama teaches a portable information terminal(paragraphs 85, 197 and 325).

7. Claims 9-10, 17-18, 28-29 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama(2002-0154151) in view of Nishioka et al(5,390,293) and Okuda(6,380,689).

As to claims 9-10, 17, 18, 28-29 and 36-37, Koyama teaches the frame period is composed of two periods of a writing period(T_a), a display period(T_s)(see figure 1 and paragraph 248).

Koyama as modified fail to disclose an erasing period.

Okuda teaches a frame period comprising three periods of writing period(address period); a display period(emission period) and an erasing period(reset period)(see figures 4, 7-8 and column 4, lines 48-53). It would have been obvious to have modified Koyama as modified with the teaching of Okuda, so as to clear previous display images.

Response to Arguments

8. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kudo et al(6,084,561) teach an LCD display for converting frame frequency.

Hirota et al(20040140972) teach a display for both n-bit gradation display and the 1-bit gradation display.

Matsueda(20020041278) teaches an OLED display having a color display mode and a monochrome display mode.

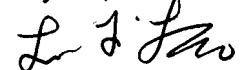
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671.

The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 18, 2007



Lun-yi Lao
Primary Examiner